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EXAMINER	
MOORE, IAN N	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/662,077	MARTIN ET AL.	
	Examiner	Art Unit	
	Ian N Moore	2661	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-23 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-22 is/are rejected.

7)☒ Claim(s) 23 is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments filed 5/21/2004 have been fully considered but they are not persuasive.

Regarding claims 1-22, the applicant argued that, "...the office action has failed to point out those portion of Edholm'269 being asserted as a "programmable audio processor chip..." and "...the portion of the Edholm'269 reference cited in support teaching for an ASIC (col. 13, line 15-17) refers to claim 4..." in page 8, paragraph 4.

In response to applicant's argument, the examiner respectfully disagrees that the office action has failed to point out those portion of Edholm'269 being asserted as a "programmable audio processor chip". As stated in office action, on **page 3, paragraph 3**, where **claim rejection for 1 and 14, clearly** stated **col. 13, line 15-17**, where examiner asserts an ASIC chip within IP telephone as programmable audio processor chip since the components within ASIC are programmed to perform, operate, and process the voice data.

Moreover, applicant is arguing that there is no cited portion of examiner assertion regarding the chip. At the same time, the applicant is admitting that the limitation was cited under Edholm'269's claim 4.

The applicant argued that, "...Edholm'269 does not teach...a programmable audio processor chip..." in page 9, last paragraph 2.

In response to applicant's argument, the examiner respectfully disagrees that the Edholm'269 does not teach a programmable audio processor chip. As applicant's admission, it was disclosed in Edholm'269 col. 13, line 15-17, as " IP telephone for use with a network is

housed in an ASIC". Moreover, it is well known in the art that, ASIC chip includes a field programmable gate array, which allow one to program ASIC. See Longacre, JR (U.S. 20030197063).

The applicant argued that, "...Edholm'269 simply states in claim 4 that certain components may be housed in an ASIC...no further support for such an ASIC implementation can be found in Edholm'269..." in page 9, last paragraph 2.

In response to applicant's argument, as applicant clearly point out in page 7, paragraph 2 that "the claims are considered part of the speciation", thus examiner believes that Edholm'269's claim 4 is part of the specification. Moreover, **the examiner respectfully disagrees that** Edholm'269 only disclose, "**certain components** may be housed in an ASIC". As clearly stated in see col. 12, lines 59 to col. 13, lines 4, Edholm'269 disclose that the components of IP telephone a controller which comprises a finite state machine, a memory, a packetizer, and network interface. The word "certain components" is not mentioned anywhere in cited pages and paragraphs.

The applicant argued that, "...Edholm'269 does not teach processing various types of compressed data as programmed (and reprogrammed)..." in page 9, paragraph 2.

In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., processing various types of compressed data as programmed (and reprogrammed)) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

The applicant argued that, "...Edholm'269 fails to assert, that the extractor 322 would be included on the claimed ASIC..." in page 9, paragraph 3.

In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., **extractor**) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

In response to applicant's arguments, the recitation "**a programmable audio processor chip**" in claim 1 has not been given patentable weight because the recitation occurs in the preamble. A preamble is generally not accorded any patentable weight where it merely recites the purpose of a process or the intended use of a structure, and where the body of the claim does not depend on the preamble for completeness but, instead, the process steps or structural limitations are able to stand alone. See *In re Hirao*, 535 F.2d 67, 190 USPQ 15 (CCPA 1976) and *Kropa v. Robie*, 187 F.2d 150, 152, 88 USPQ 478, 481 (CCPA 1951).

Moreover, it is inherent that since the packetizer is on the chip, the extractor must also be on the chip since they both process the IP packet. Since the claimed limitation only neither recites a packetizer nor the extractor, examiner asserts that they both are IP stack.

The applicant argued that, "...the office action failed to show how a DSP could be integrated with asserted ASIC of the Edholm'269 reference..." in page 9, paragraph 3, "...the office action failed to include any evidence from the prior art in support of these allegations..." in page 10, paragraph 2, and "...how such an integrated DSP would function

in connection with Edholm'269 as apparently combined with the ASIC..." page 10, paragraph 2.

In response to applicant's argument, the examiner respectfully disagrees that the office action failed to show how a DSP could be integrated with asserted ASIC. As disclose in the office action, it is well known in the art that, a chip comprises DSP, and DSP is implemented on any device, which process data. The following lists prior arts that clearly show the evidence that DSP is integrated on the chip or ASIC.

i. Raman, US 5,400,394- Abstract- voice/audio a digital signal processor (DSP) chip

ii. Dean, US 5,303,326- Abstract- audio a digital signal processor (DSP) chip

iii. Nakagawa, US 6,353,863- Abstract- a DSP/CPU integrated chip

iv. Baji, US 5,513,374- Abstract- a single chip digital signal processor DSP includes on-chip memory and controller

Thus, it is clear from the well-established teaching in art from the list of references that a DSP is implemented on the chip (i.e. ASIC). Edholm'269 teaches VoIP components on the ASIC chip. The well known (i.e. newly cited prior arts) teaches that DSP is on the chip. Thus, it is clear to one skill in the ordinary art to integrate DSP on the chip or ASIC for the purpose of reducing the size of the VoIP telephone. The motivation being that, as recited in previous office action, by integrating or incorporating all the VoIP components into a chip, it would make the VoIP phone smaller since user constantly demands smaller and compact telephony device, which is easy to carry and store.

The applicant argued that, "...the office action failed to show any teaching or suggestion of these limitations...to dissipate as claim 9 is directed..." in page 9, paragraph 3.

In response to applicant's argument, the examiner respectfully disagrees that the office action failed to show any teaching or suggestion of these limitations...to dissipate as claim 9 is directed. As disclose in the office action, it is well known in the art that, a chip dissipate 250 mW at 200 MHz. The following lists prior arts that clearly show the limitations.

v. Sugiura, US 4,248,200- see col. 11, lines 1-2- the total thermal capacity of IC is about 250 mW.

vi. Yoder, US 6,456,138- see col. 1, lines 49-51- a pipleline logic chip operating at 200 MHz

vii. Waggoner, US 6,218,706- see col. 10, lines 33-36- 200 MHz for use in high speed IC

viii. DaSilva, US 5,694,093- abstract- a GaAs IC for use in 200 MHz

Thus, it is clear from the well-established teaching in art from the list of the references that the chip (i.e. ASIC) can dissipate at 250 mW at 200 MHz. In particular, a chip can be designed to dissipate 250 mW at 200 MHz or any variation as long as it gives the minimum power dissipation for ASIC. By minimizing ASIC's power dissipation, it will produce small amount of heat and/or consume small amount power (i.e. for battery powered mobile/cordless VoIP phones). The art of reducing the battery power consumption for a mobile/cordless phone in order for the user to utilize the phone battery longer without re-charging is also well known in the art of mobile/cordless telephone. Also, it is also well

known in the art that ASIC can also operate at 200 MHz with benchmark performance of power dissipation. In view of this, having the system of Edholm'269 and then given well known teaching in the art, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the system of Edholm'269, by setting the power dissipation at 250 mW at 200 MHz. The motivation to combine is to obtain the advantages/benefits taught by well-established teaching in the art that such modification would make it possible to minimize the power dissipation of ASIC by setting lower power at higher frequency so that it will produce less heat during active operation. It also is well known in the art it constantly demands longer battery life for a battery powered telephony device so that the user can be utilized without re-charging frequently. In order to extend the battery life and reduce heat, the power dissipation of the ASIC inside the phone must be minimized.

The applicant argued that, "...CPU that programs **the (external) IP telephony device**...it is unclear as to how the controller 314 could function both as the claimed audio processing circuitry of an IP telephone and as a CPU adapted to communicate with the IP telephone..." in page 9, paragraph 5 and "...the skilled artisan would recognized that the CPU is **outside** the telephony device and another aspect of the claimed network..." in page 8, paragraphe 2.

In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., CPU is **outside the telephony device or the external IP telephony device**) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations

from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

In response to applicant's argument, Edholm'269 teaches a controller which process a state finite machine to compress voice data, see col. 2, lines 47-51, see col. 8, lines 30-57, FIG.3 and 4. Thus, examiner asserts a controller as the audio processing circuitry. Also, Edholm'269 teaches a controller which function as a central processor unit to process memory 332-extractor 322-packetizer 334, mac 328, and etc. see FIG. 3. and previous office action page 11. The same controller communicates with plurality of telephony device via network 130, see col. 8, lines 30 to col. 9, lines 55. Thus, examiner asserts a controller as a central processing unit since it processes and controls internal components and communicates with other telephony devices. Thus, it is clear that Edholm'269's controller can perform multiple processes. Edholm'269 teaches the plurality of IP telephony devices, and each device contains a CPU, see FIG. 1, IP telephone 100, and a computer 170 with microphone 172 and speaker 171; see col. 4, lines 55 to col. 5, lines 9. Thus, examiner asserts Edholm'269's the controller from an IP telephone device (e.g. IP phone 100) and adapted to communicate with other IP telephone devices (i.e. a computer 170 with microphone 172 and speaker 171), which carry VoIP traffic.

The applicant argued that, "...Edholm'269 cannot ascertain where the controller 314 would be programmable by a CPU as claimed..." in page 10, paragraph 1.

In response to applicant's argument, the examiner respectfully disagrees that Edholm'269 cannot ascertain where the controller 314 would be programmable by a CPU as claimed. Note that Edholm'269 discloses the one IP telephony device is setting/programming

a communication path (i.e. call connection set-ups or tear down utilizing H.323) with the other IP telephony device. Thus, it is clear that the controller 314 from one IP telephony device can set or program the communication path to the controller 312 in the other IP telephony device; see col. 8, lines 30 to col. 9, lines 56).

The applicant argued that, "...the office action failed to show how one of skill in the art would be motivated to modify and **reprogram the application-specific programmed controller 314** of the Edholm'269 with new, external programming via the flash-cache architecture.

In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., **reprogram the application-specific programmed controller and new, external programming**) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

In response to applicant's argument, the motivation to modify the combined system of Edholm'269 and well-established teaching in the art, for the purpose of providing a microcomputer/chip which has a mechanism to execute user boot programs from the flash memory and store the programs into RAM, as taught by Maeda'074. The motivation to combine is to obtain the advantages/benefits taught by Maeda'074 since Maeda'074 states at col. 1, line 64-66 that such modification would make it possible to provide a microcomputer/chip capable of releasing the entire area of the flash memory for a user program area.

In view of the above, **the examiner respectfully disagrees** with applicant's argument and believes that the combination of references as set forth in the 103 rejections is proper, thus, Claims 1-22 are obvious over Edholm'269 in view of well established teaching in art for at least the reasons discussed above.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

1. Claims 1-9 and 13,14, and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Edholm (U.S. 6,449,269) in view of well-established teaching in the art.

Regarding claim 1 and 14, Edholm'269 discloses a DSP voice compression device (see FIG. 3, DSP 310) adapted to compress the voice data (see col. 5, line 56 to col. 6, line 14; note that the digitized voice signals are compressed utilizing H.323 compressing techniques.), and a programmable audio processor chip for processing voice data (see col. 13, line 15-17, an ASIC, Application Specific Integrated Circuit; note that the components within ASIC are program to perform, operate, and process the voice data; therefore ASIC is programmable chip.) comprising:

audio processing circuitry (see FIG. 3, Controller 314) programmed with an audio processing software application for processing the compressed voice data (see col. 2, line 47-

51; col. 8, line 30-57; note that a controller comprises the finite state machine (i.e. application) to process compressed voice data; also see FIG. 4);

an IP network stack (see FIG. 3, a combined system of Packetizer 334, memory 332, and Extractor 322) adapted to store and process IP data, the IP data including protocols for processing the compressed voice data via an IP network (see col. 6, line 14-29, col. 7, line 54-67; note that the packetizer packetizes/processes the digitized voice data into IP packets, the memory stores/maintains the IP address information, and the extractor extracts/processes the digitized voice from the IP packets which are received from the network which are received from the network); and

a communication stack (see FIG. 3, a combined system of Controller 314, Packetizer 334 and memory 332) adapted to store and process communications data, the communications data including audio processing protocols for processing the compressed voice data (see col. 8, line 30 to col. 9, line 56; not that the controller instructs/processes the packetizer to establish call connection setup and terminates the call after on-hook; the memory stores/maintains/flushes the IP address information).

Edholm'269 does not explicitly disclose a chip comprises DSP voice compression device.

However, the above-mentioned claimed limitations are well known in the art of telephony and integrated circuitry. In particular, a chip can be designed to include DSP voice compression device.

In view of this, having the system of Edholm'269 and then given well known teaching in the art, it would have been obvious to one having ordinary skill in the art at the time the

invention was made to modify the system of Edholm'269, by including the DSP on the ASIC. The motivation to combine is to obtain the advantages/benefits taught by well-established teaching in the art that such modification would make it possible to reduce the size of the VoIP telephone by including a DSP on the ASIC. It also is well known in the art that the user constantly demands smaller and compact telephony device, which is easy to carry and store, and the only way to meet user demand is by utilizing ASIC technology.

Regarding claim 2, the combined system of Edholm'269 and well-established teaching in art discloses the programmable audio processor as described above in Claim 1.

Moreover, Edholm'269 discloses the chip is further adapted to convert the voice data between IP audio data and digital audio data (see FIG. 3, Packetizer 334; also see col. 6, line 1-38; note that Packetizer packetizes/converts between the digitized compressed voice signals/data (from DSP) into IP packet/data).

Regarding claim 3, the combined system of Edholm'269 and well-established teaching in art discloses the programmable audio processor as described above in Claim 1.

Moreover, Edholm'269 discloses an analog-digital (A/D) converter (see FIG. 3, A/D 304) adapted to convert the voice data between analog and digital form (see col. 5, line 56 to col.6, line 3).

Regarding claim 4, the combined system of Edholm'269 and well-established teaching in art discloses the A/D converter as described above in Claim 3.

Moreover, Edholm'269 discloses the A/D converter is adapted to convert voice data captured at a microphone (see FIG. 3, Microphone 302) of a telephony device (see FIG. 3, IP phone 100) employing the audio processor and to deliver the converted signal to the audio data converter (see col. 6, line 5-13; the A/D converter converts the voice signals, captured by the microphone, and transmits towards DSP for audio data compressing).

Regarding claim 5, the combined system of Edholm'269 and well-established teaching in art discloses the A/D converter as described above in Claim 3.

Moreover, Edholm'269 discloses a telephony device (see FIG. 3, IP phone 100) that houses the audio processor, wherein the A/D converter is adapted to convert a digital signal received from the converter into analog form for use at a speaker of the telephony device (see FIG. 3, Speaker 302 and Sound Generator 306; note that a digitized data are transmitted by the controller into a speaker via A/D converter and sound generator in order to reconstruct analog voice signals.)

Regarding claim 6, the combined system of Edholm'269 and well-established teaching in art discloses the programmable audio processor as described above in Claim 1.

Moreover, Edholm'269 discloses wherein IP network stack includes at least one of: a TCP/IP stack and a H.323 stack (see col. 11, line 11-26, and col. 12, line 1-12; note that Edholm'269's IP telephony device utilizes TCP/IP and/or ITU H.323 signaling. Moreover, the packetizer utilizes TCP/IP scheme of packetizing.)

Regarding claim 7, the combined system of Edholm'269 and well-established teaching in art discloses the programmable audio processor as described above in Claim 1.

Moreover, Edholm'269 discloses wherein the communication stack is adapted to provide at least one of the following protocols: call setup, call tear down, capabilities exchange and negotiation (see col. 8, line 30 to col. 9, line 56; not that the controller instructs/processes the packetizer to establish call connection setup and terminates/tear down the call after on-hook.)

Regarding claim 8, the combined system of Edholm'269 and well-established teaching in art discloses the programmable audio processor as described above in Claim 1.

Moreover, Edholm'269 discloses sufficient on-chip RAM (see FIG. 3, Memory 332) to run a connection-less thin client call stack (see col. 6, line 16-65; note that packetizer set up connection for a call utilizing the memory.) a TCP/IP stack (see col. 12, line 1-11; the controller utilizes memory for TCP/IP for signaling.) and audio compression protocols (see Fig. 4, and col. 8, line 31 to col. 9, line 56; the controller utilizes memory to process digitized compressed voice data and IP packet data.), wherein the processor is adapted to function without external system memory (see FIG. 3, Memory 332; note that there is only one on-board memory on ASIC and all operations are performed utilizing this memory.)

Regarding claim 9, Edholm'269 discloses wherein the chip is adapted to dissipate 250 mW at 200 MHz.

Edholm'269 does not explicitly wherein the chip is adapted to dissipate 250 mW at 200 MHz.

However, the above-mentioned claimed limitations are well known in the art of telephony and integrated circuitry. In particular, a chip can be designed to dissipate 250 mW at 200 MHz or any variation as long as it gives the minimum power dissipation for ASIC. By minimizing ASIC's power dissipation, it will produce small amount of heat and/or consume small amount power (i.e. for battery powered mobile/cordless VoIP phones). The art of reducing the battery power consumption for a mobile/cordless phone in order for the user to utilize the phone battery longer without re-charging is also well known in the art of mobile/cordless telephone. Also, it is also well known in the art that ASIC can also operate at 200 MHz with benchmark performance of power dissipation.

In view of this, having the system of Edholm'269 and then given well known teaching in the art, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the system of Edholm'269, by setting the power dissipation at 250 mW at 200 MHz. The motivation to combine is to obtain the advantages/benefits taught by well-established teaching in the art that such modification would make it possible to minimize the power dissipation of ASIC by setting lower power at higher frequency so that it will produce less heat during active operation. It also is well known in the art it constantly demands longer battery life for a battery powered telephony device so that the user can be utilized without re-charging frequently. In order to extend the battery life and reduce heat, the power dissipation of the ASIC inside the phone must be minimized.

Regarding Claim 13, Edholm'269 discloses a telephony communications device (see FIG. 3, IP phone 100) adapted to communicate data including voice data, the device comprising:

DSP functions (see FIG. 3, DSP 310) and a programmable audio processor chip having microcontroller functions (see FIG. 3, a combined system of Controller 314, Packetizer 334, Extractor 322, and Memory 332) and adapted to perform Internet protocol/digital (IP/D) conversions for IP voice data and digital voice data (see col. 6, line 14-39; note that the packetizer latches/transforms/converts digitized voice signals into IP packets.)

an audio capture device communicatively linked to the programmable audio processor chip (see FIG. 3, Microphone 302) and adapted to capture voice data and communicate the captured voice data to the programmable audio processor chip (see col. 6, line 5-13; the voice signals are captured by the microphone and transmits towards DSP via A/D converter); and

an audio speaker communicatively linked to the programmable audio processor chip (see FIG. 3, Speaker 302) and adapted to generate sound (see FIG. 3, Sound Generator 306) in response to data communicated from the programmable audio processor chip (see col. 5, line 56 to col.6, line 2; a digitized data are transmitted by the controller into a speaker via A/D converter and sound generator in order to reconstruct analog voice signals.)

Edholm'269 does not explicitly disclose a chip having DSP function.

However, the above-mentioned claimed limitations are well known in the art of telephony and integrated circuitry. In particular, a chip can be designed to include DSP functional device.

In view of this, having the system of Edholm'269 and then given well known teaching in the art, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the system of Edholm'269, by including the DSP on the ASIC. The motivation to combine is to obtain the advantages/benefits taught by well-established teaching in the art that such modification would make it possible to reduce the size of the VoIP telephone by including a DSP on the ASIC. It also is well known in the art that the user constantly demands smaller and compact telephony device, which is easy to carry and store, and the only way to meet user demand is by utilizing ASIC technology.

Regarding Claim 20, Edholm'269 discloses an IP telephony communications network (see FIG. 1, IP telephony network) comprising:

a plurality of IP telephony devices (see FIG. 1, plurality of IP phones 100 and 171) each having a DSP voice compression device (see FIG. 3, DSP 310) adapted to compress the voice data (see col. 5, line 56 to col. 6, line 14; note that the digitized voice signals are compressed utilizing H.323 compressing techniques.), and a programmable audio processor chip for processing voice data (see col. 13, line 15-17, an ASIC, Application Specific Integrated Circuit; note that the components within ASIC are program to perform, operate, and process the voice data; therefore ASIC is programmable chip.) comprising:

audio processing circuitry (see FIG. 3, Controller 314) programmed with an audio processing software application for processing the compressed voice data (see col. 2, line 47-51; col. 8, line 30-57; note that a controller comprises the finite state machine (i.e. application) to process compressed voice data; also see FIG. 4);

an IP network stack (see FIG. 3, a combined system of Packetizer 334, memory 332, and Extractor 322) adapted to store and process IP data, the IP data including protocols for processing the compressed voice data via an IP network (see col. 6, line 14-29, col. 7, line 54-67; note that the packetizer packetizes/processes the digitized voice data into IP packets, the memory stores/maintains the IP address information, and the extractor extracts/processes the digitized voice from the IP packets which are received from the network); and

a communication stack (see FIG. 3, a combined system of Controller 314, Packetizer 334 and memory 332) adapted to store and process communications data, the communications data including audio processing protocols for processing the compressed voice data (see col. 8, line 30 to col. 9, line 56; not that the controller instructs/processes the packetizer to establish call connection setup and terminates the call after on-hook; the memory stores/maintains/flushes the IP address information);

a CPU (see FIG. 3 Controller 314) adapted to communicate with the plurality of IP telephony communications devices and to program the programmable audio processor chip in each IP telephony device (see FIG. 1 and col. 8, line 30 to col. 9, line 55; note that the controller communicates with plurality of phones 100, 171, 160, Phone server 110, via network 130; and the controller controls/programs to perform the devices on the ASIC (i.e. memory, packetizer, extractor) and processes the operation according to the programmed

finite state machine.), the programming including communications protocols, the CPU adapted to execute a plurality of instructions simultaneously (see col. 8, line 30 to col. 9, line 56; note that the controller executes the instruction for the packetizer to establish call connection setup and terminates/tear down the call after on-hook, utilizing the TCP/IP and/or ITU H.323 communication signaling. Moreover, the packetizer utilizes TCP/IP scheme of packetizing. The controller executes/processes the plurality of instruction/functions according to the state diagram, see FIG. 4 and 6); and

a communications link coupled to each of the IP telephony devices and to the CPU and adapted to transmit communications data including voice IP data (see FIG. 1, the communication links between the controller 314 of IP phone 100, IP PC phone 170, and network 130; also see col. 4, line 21 to col. 5, line 9; note that VoIP data are transmitted/received to/from the other VoIP phone via the network.)

Edholm'269 does not explicitly disclose a chip comprises DSP voice compression device and the CPU having a standard RISC 5-stage pipeline.

However, the above-mentioned claimed limitations are well known in the art of telephony and integrated circuitry. In particular, a chip can be designed to include DSP voice compression device. The CPU can be designed with a standard RISC 5-stage pipeline.

In view of this, having the system of Edholm'269 and then given well known teaching in the art, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the system of Edholm'269, by including the DSP on the ASIC and designing the CPU according to the standard. The motivation to combine is to obtain the advantages/benefits taught by well-established teaching in the art that such modification

would make it possible to reduce the size of the VoIP telephone by including a DSP on the ASIC. It also is well known in the art that the user constantly demands smaller and compact telephony device, which is easy to carry and store, and the only way to meet user demand is by utilizing ASIC technology. Moreover, by designing the standardized CPU, it will enable to inter-operate with the other CPU or devices.

2. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Edholm'269 and well-known teaching in the art as applied to claim 1 above, and further in view of Bertin (U.S. 6,097,243).

Regarding claim 10, the combined system of Edholm'269 and well-established teaching in art discloses the programmable audio processor circuitry as described above in Claim 1.

The combined system does not explicitly disclose wherein the circuitry is in a power-down mode, wherein the internal clock frequency is slowed during periods of chip inactivity.

However, the above-mentioned claimed limitations are taught Bertin'243. In particular, Bertin'243 teaches wherein the circuitry is in a power-down mode, wherein the internal clock frequency is slowed during periods of chip inactivity (see col. 2, line 54 to col. 3, line 45; note that in order to reduce power consumption the semiconductor device is put into a groggy mode (i.e. power-down mode) by reducing operational clock speed during inactivity).

In view of this, having the combined system of Edholm'269 and well-established teaching in the art, then given the teaching of Bertin'243, it would have been obvious to one

having ordinary skill in the art at the time the invention was made to modify the combined system of Edholm'269 and well-established teaching in the art, by providing a mechanism to reduce the clock speed during inactivity, as taught by Bertin'243. The motivation to combine is to obtain the advantages/benefits taught by Bertin'243 since Bertin'243 states at col. 2, line 54-56 that such modification would make it possible to reduce power consumption while maintaining full functionality of the semiconductor device.

3. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Edholm'269 and well-known teaching in the art as applied to claim 1 above, and further in view of Mason (U.S. 6,272,451).

Regarding claim 11, the combined system of Edholm'269 and well-established teaching in art discloses the programmable audio processor circuitry as described above in Claim 1.

The combined system does not explicitly disclose wherein the circuitry is adapted to be programmed using C programming language.

However, the above-mentioned claimed limitations are taught Mason'451. In particular, Mason'451 teaches wherein the circuitry is adapted to be programmed using C programming language (see col. 9, line 19-29; note that FPGA microcontroller designs are usually done in the C-language).

In view of this, having the combined system of Edholm'269 and well-established teaching in the art, then given the teaching of Mason'451, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the combined

system of Edholm'269 and well-established teaching in the art, by providing a mechanism to program the circuitry/chip with C-programming language, as taught by Mason'451. The motivation to combine is to obtain the advantages/benefits taught by Mason'451 since Mason'451 states at col. 4, line 66 to col. 5, line 10 that such modification would make it possible to allow programmable logic users to design, with ease, FPSLIC devices which contain microprocessors by utilizing software tool.

4. Claim 12 and 15-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Edholm'269 and well-known teaching in the art as applied to claim 1 and 13 above, and further in view of Maeda (U.S. 5,884,074).

Regarding claims 12 and 15, the combined system of Edholm'269 and well-established teaching in art discloses telecommunication device comprising the programmable audio processor circuitry as described above in Claim 1 and 13. Furthermore, Edholm'269 discloses a CPU (see FIG. 3, Controller) and execution space with memory on the chip (see col. 6, line 16-65; col. 12, line 1-11; Fig. 4, and col. 8, line 31 to col. 9, line 56; note that the controller executes memory for packetizing, TCP/IP for signaling, and processing of digitized voice.)

The combined system does not explicitly discloses the flash-style, non-volatile memory, that includes embedded firmware for that device and wherein the circuitry of the Flash-cache architecture adapted to enable a CPU to boot and run code from an external Flash-style device, and mix this execution space with memory.

However, the above-mentioned claimed limitations are taught Maeda'074. In particular, Maeda'074 teaches the flash-style, non-volatile memory (see FIG. 1, Flash Memory 11), that includes embedded firmware for that device and wherein the circuitry of Flash-cache architecture adapted to enable a CPU (see FIG. 1, CPU 17) to boot and run code from an external Flash-style device (see FIG. 1, Flash Memory 11; note that CPU executes the boot program stored in the boot program area of the flash memory), and mix this execution space with memory (see FIG. 1, RAM 2; see col. 1, line 20 to col. 2, line 22; note that CPU stores programs in the RAM. Thus, it is clear that combined memories from both memory units (i.e. Flash and RAM) must be utilized for CPU execution).

In view of this, having the combined system of Edholm'269 and well-established teaching in the art, then given the teaching of Maeda'074, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the combined system of Edholm'269 and well-established teaching in the art, by providing a microcomputer/chip which has a mechanism to execute user boot programs from the flash memory and store the programs into RAM, as taught by Maeda'074. The motivation to combine is to obtain the advantages/benefits taught by Maeda'074 since Maeda'074 states at col. 1, line 64-66 that such modification would make it possible to provide a microcomputer/chip capable of releasing the entire area of the flash memory for a user program area.

Regarding claim 16, the combined system of Edholm'269, well-established teaching in art and Maeda'074 discloses the telephony communications device, further comprising a

plurality of communications stacks, DSP codes, RAM and external flash memory as described above in Claims 1 and 13-15.

Furthermore, Edholm'269 teaches the device (see FIG. 3, Controller) adapted to run compute-intensive DSP code and to run the communication stacks out of memory (see col. 6, line 16-65; col. 12, line 1-11; Fig. 4, and col. 8, line 31 to col. 9, line 56; note that the controller executes memory for processing of digitized voice (i.e. running DSP code), packetizing and TCP/IP for signaling (i.e. running communication stacks)). In addition Maeda'074 discloses the device (see FIG. 1, CPU 17) is adapted to run programs/instructions/tasks from an external flash memory as described above in Claim 15.

Neither Edholm'269 nor Maeda'074 explicitly discloses the device is adapted to run compute-intensive DSP code out of internal RAM and to run the communication stacks out of external flash memory.

However, the above-mentioned claimed limitations are well known in the art. In particular, the device can be adapted to run compute-intensive DSP code out of internal RAM and to run the communication stacks out of external flash memory. Edholm'269 teaches a device which all computations and processes will be utilized/run by the single memory. Maeda'074 also teaches utilizing the flash memory to run/boot the user-defined programs and RAM to store programs. Thus, it is obvious and well known in the art that the computational functions and processes can be divided/distributed between various type memories (i.e. RAM vs. ROM/Flash-memory) in any computer related device. Thus, Flash memory can be used to boot and run the programs to set up the TCP/IP communication, and RAM memory can be used to store programs for DSP and packetizing devices.

In view of this, having the combined system of Edholm'269 and Maeda'074, then given well known teaching in the art, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the combined system of Edholm'269 and Maeda'074, by assigning specific function for each type of memories. The motivation to combine is to obtain the advantages/benefits taught by well-established teaching in the art that such modification would make it possible to avoid process overloading in computer related device by assigning the computational and processing load among memory units.

Regarding claim 17, the combined system of Edholm'269, well established teaching in art and Maeda'074 discloses the telephony communications device as described above in Claims 13. Furthermore, Edholm'269 teaches the device is adapted to run DSP code including at least one of: audio codecs, acoustic echo cancellation and framing (see col. 6, line 1-12; note that DSP encode and decode the digitized voice by using echo cancellation procedures.)

Regarding claim 18, the combined system of Edholm'269 well established teaching in art and Maeda'074 discloses the programmable audio processor as described above in Claim 16.

Moreover, Edholm'269 discloses wherein the communication stack is adapted to provide at least one of the following protocols: call setup, call tear down, capabilities exchange and negotiation (see col. 8, line 30 to col. 9, line 56; not that the controller

instructs/processes the packetizer to establish call connection setup and terminates/tear down the call after on-hook.)

5. Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over Edholm'269 and well-known teaching in the art as applied to claim 13 above, and further in view of Blomley (U.S. 4,608,462).

Regarding claim 19, the combined system of Edholm'269 and well-established teaching in art discloses the chip as described above in Claim 13.

The combined system of Edholm'269 does not explicitly disclose the chip includes a chip set having a plurality of chips, each of the plurality of chips being adapted to perform at least one selected function of the chip.

However, the above-mentioned claimed limitations are taught by Blomley'462. In particular, Blomley'462 teaches the chip includes a chip set having a plurality of chips, each of the plurality of chips being adapted to perform at least one selected function of the chip (see col. 1, line 45 to col. 2, line 29; note that an integrated circuit chip set for a telephone instrument includes first ancillary chip and second ancillary chip. Both chips perform specific/selected function of a chip).

In view of this, having the combined system of Edholm'269 and well-established teaching in the art, then given the teaching of Blomley'462, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the combined system of Edholm'269 and well-established teaching in the art, by providing a chip set which consists of plurality of chips and each chip performs specific function, as taught by

Blomley'462. The motivation to combine is to obtain the advantages/benefits taught by Blomley'462 since Blomley'462 states at col. 1, line 45 to col.2, line 15 that such modification would make it possible to minimize/overcome the limitation of utilizing CMOS and bipolar devices on a single chip by utilizing the an integrated chip set.

6. Claims 21-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Edholm'269 and well-known teaching in the art as applied to claim 20 above, and further in view of Adelman (U.S. 5,598,362).

Regarding claim 21, the combined system of Edholm'269 and well-established teaching in art discloses the CPU as described above in Claim 20.

The combined system of Edholm'269 does not explicitly disclose wherein the CPU further comprises a DSP Multiply Accumulate (DSPMAC) unit and an Address Generation Unit (AGU).

However, the above-mentioned claimed limitations are taught by Adelman'362. In particular, Adelman'362 teaches a DSP Multiply Accumulate (DSPMAC) unit (see FIG. 2, Multiplier 76 of Data Arithmetic Logic unit performing DSP multiply/accumulate (MAC) operation; see col. 1, line 29-34) and an Address Generation Unit (AGU) (see FIG. 1, Address Generation Unit 36, AGU; see col. 4, line 6-14).

In view of this, having the combined system of Edholm'269 and well-established teaching in the art, then given the teaching of Adelman'362, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the combined system of Edholm'269 and well-established teaching in the art, by providing DSP

MAC and AGU units, as taught by Adelman'362. The motivation to combine is to obtain the advantages/benefits taught by Adelman'362 since Adelman'362 states at col. 1, line 45 to col.1, line 30-55 that such modification would make it possible to provide greater voice accuracy.

Regarding claim 22, the combined system of Edholm'269, Adelman'362, and well-established teaching in art discloses the AGU and CPU as described above in Claims 20 and 21. In particular, Edholm'269 teaches the controller which performs the function of the CPU. Adelman'362 teaches AGU, which generates the address of the instruction (see col. 4, line 6-54). Also, it is well known in the art that the function of a controller/CPU is to execute instructions/tasks by calculating the address of the operand.

The combined system of Edholm'269 and Adelman'362 does not explicitly disclose wherein the AGU is adapted to effect address calculation concurrently with normal program flow address calculation of the CPU.

However, the above-mentioned claimed limitations are taught by well known in the art. In particular, the AGU is adapted to effect address calculation concurrently with normal program flow address calculation of the CPU. Note that both AGU and controller/CPU have the functionality of generating/calculating the addresses, and they are both in the same ASIC chip. Thus, it is clear that they both must calculate/generate the address in parallel manner.

In view of this, having the combined system of Edholm'269 and Adelman'362, then given the well-established teaching in the art, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the combined system of

Edholm'269 and well-established teaching in the art, by providing a mechanism for the controller/CPU and AGU units which perform the address calculation/generation in parallel manner as taught by well-established teaching in the art. The motivation to combine is to obtain the advantages/benefits taught by well-established teaching in the art since such modification would make it possible to provide faster CPU/controller processing since the tasks are now performed in parallel manner.

Allowable Subject Matter

7. Claim 23 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Notes/Remarks

8. Objections to the specification are withdrawn.

9. Claim rejection under 35 USC § 112, second paragraph, on claim 20 is withdrawn.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ian N Moore whose telephone number is 703-605-1531. The examiner can normally be reached on M-F: 9-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ken Vanderpuye can be reached on 703-308-7828. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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KENNETH VANDERPUYE
PRIMARY EXAMINER